

Figure 1

| V_{in} | i_a | i_b |
|--------------------------------|-------|-------|
| $V_{in} > V_{refH}$ | i | $2i$ |
| $V_{refH} > V_{in} > V_{refL}$ | $2i$ | i |
| $V_{in} < V_{refL}$ | i | $2i$ |

200

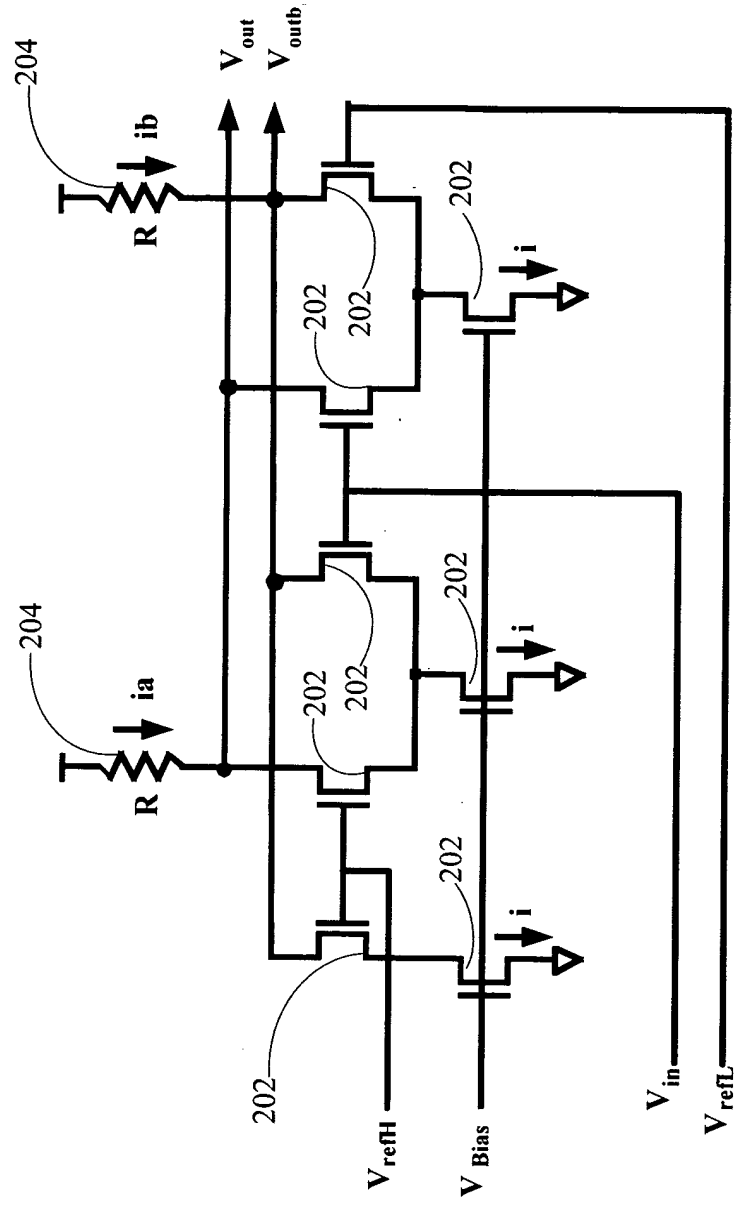


Figure 2

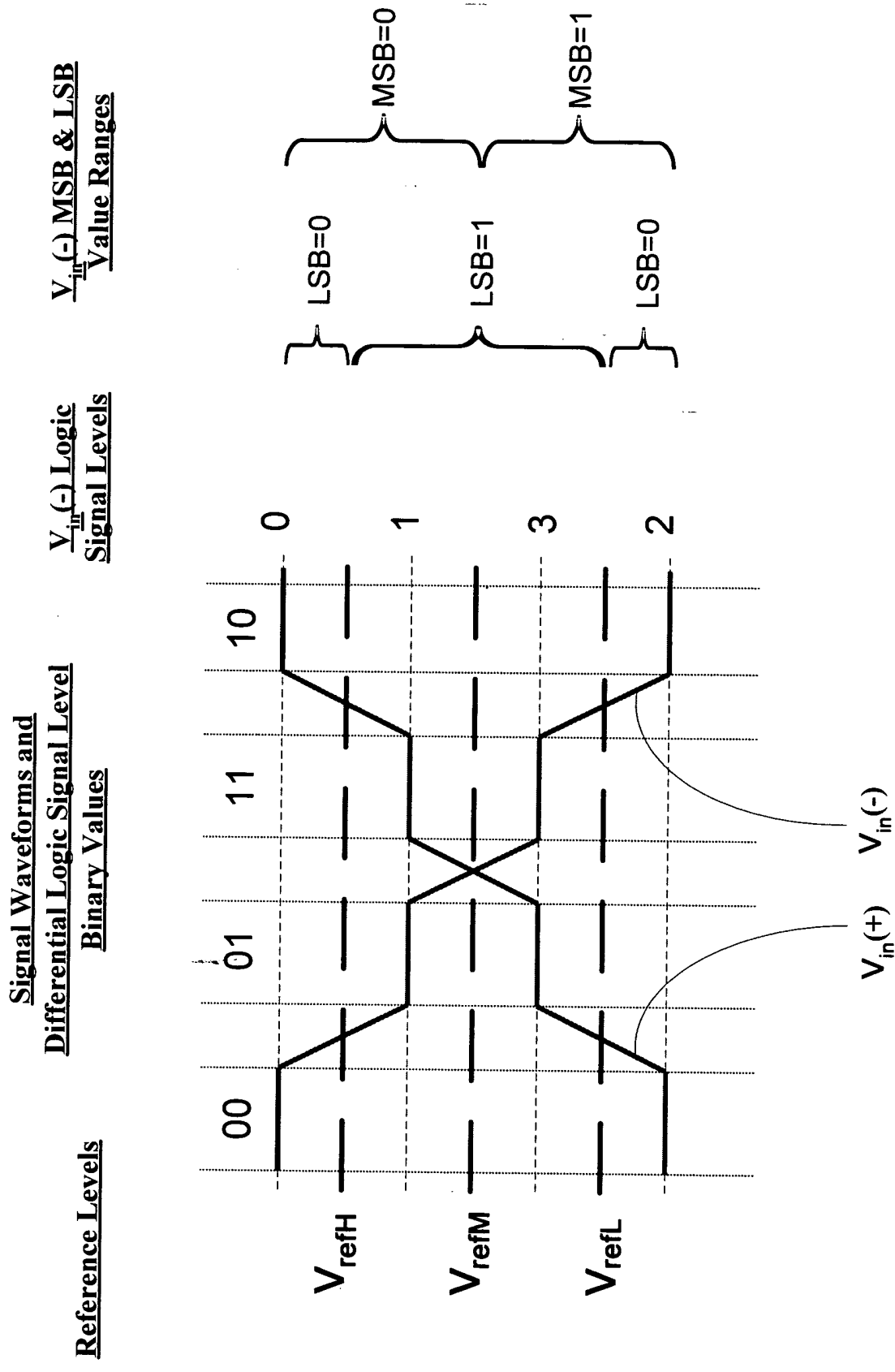


Figure 3

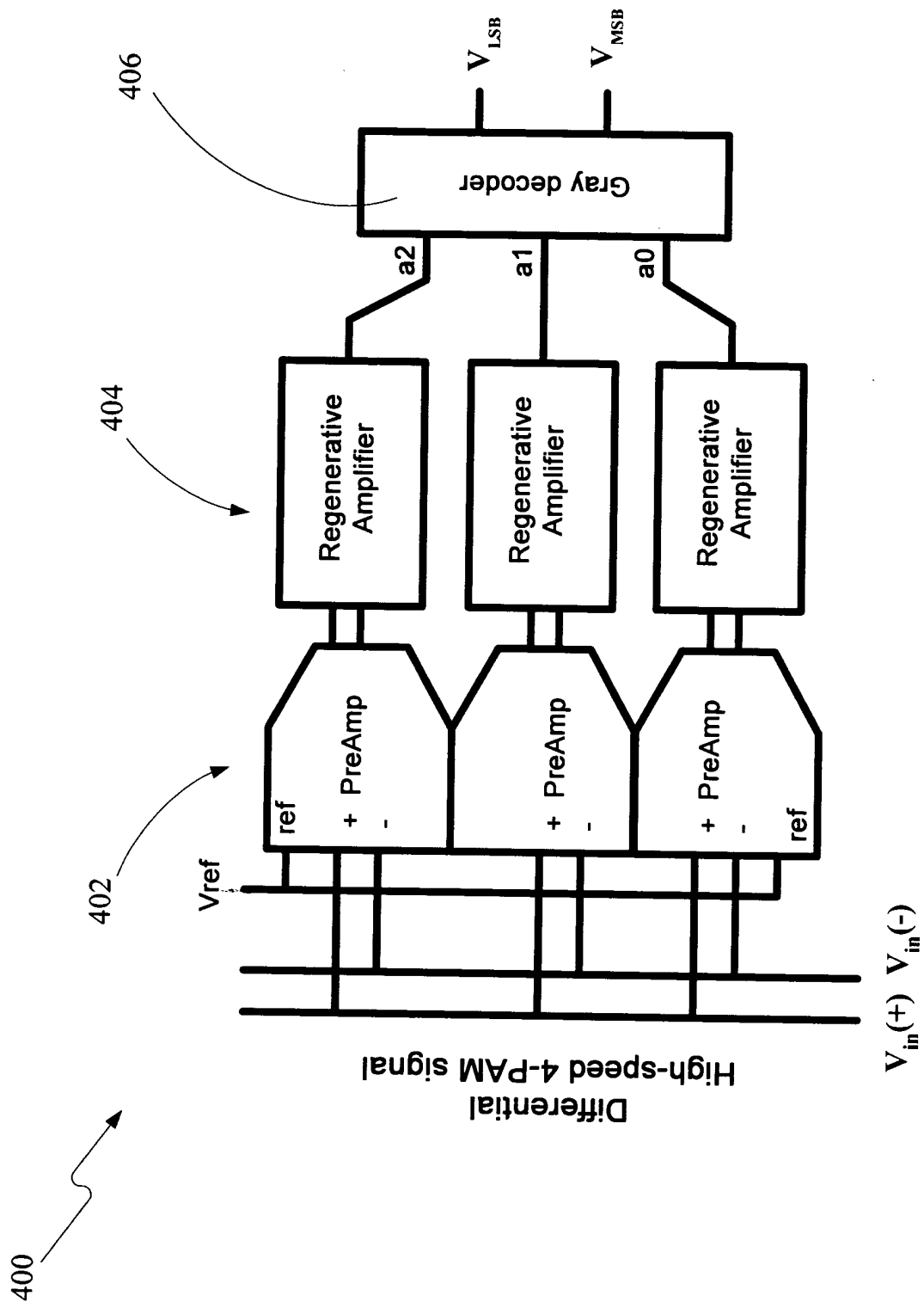


Figure 4A

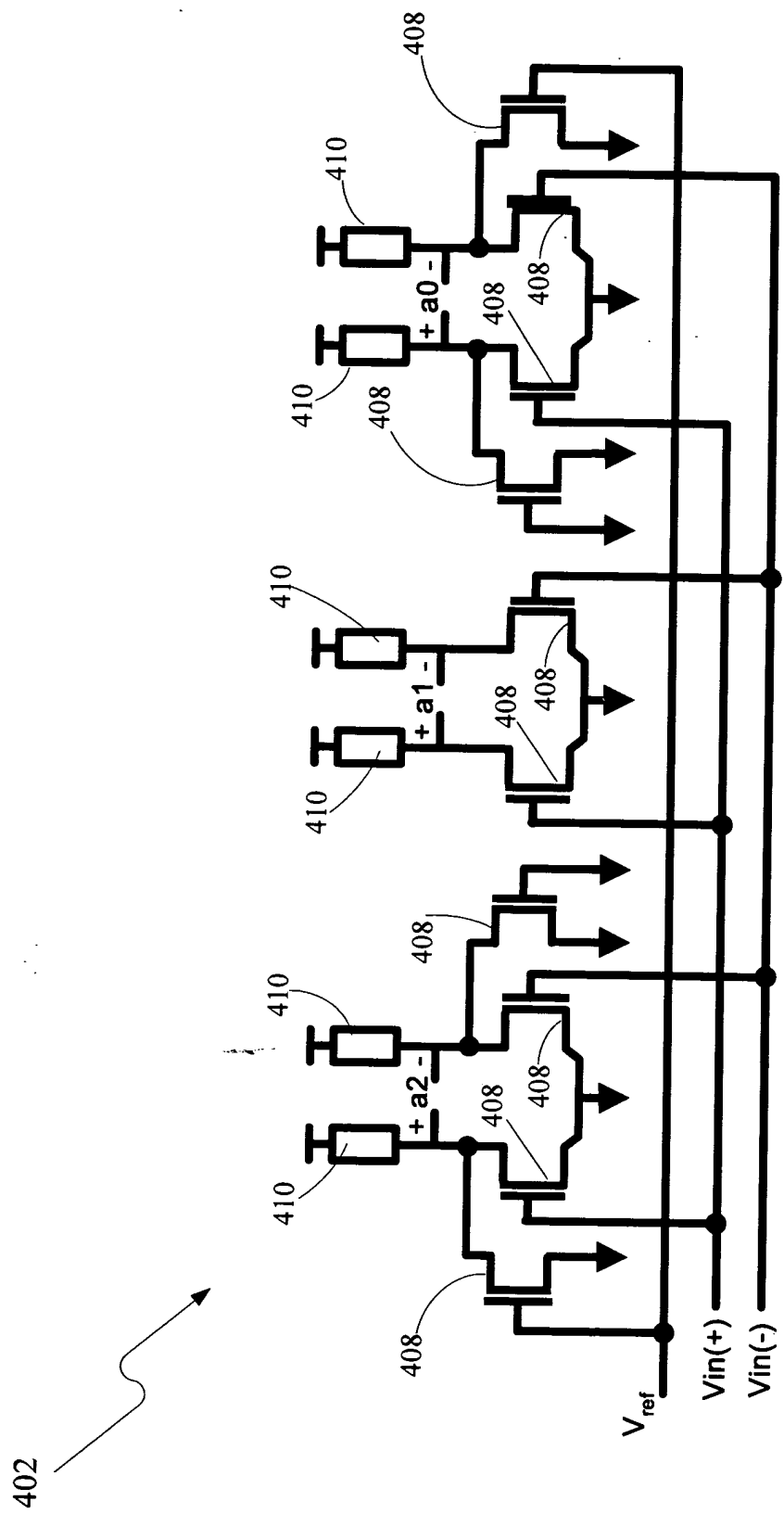


Figure 4B

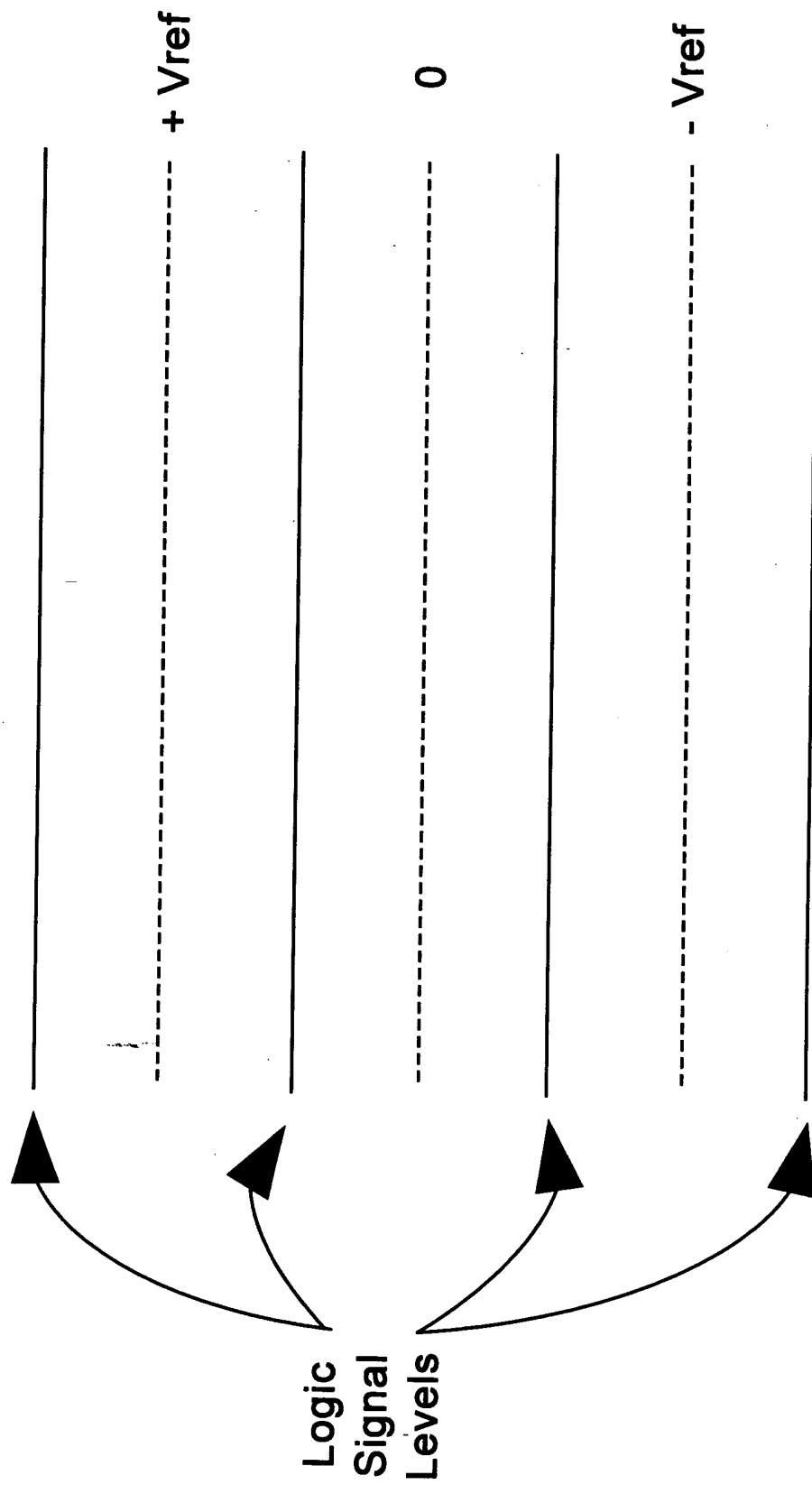


Figure 4C

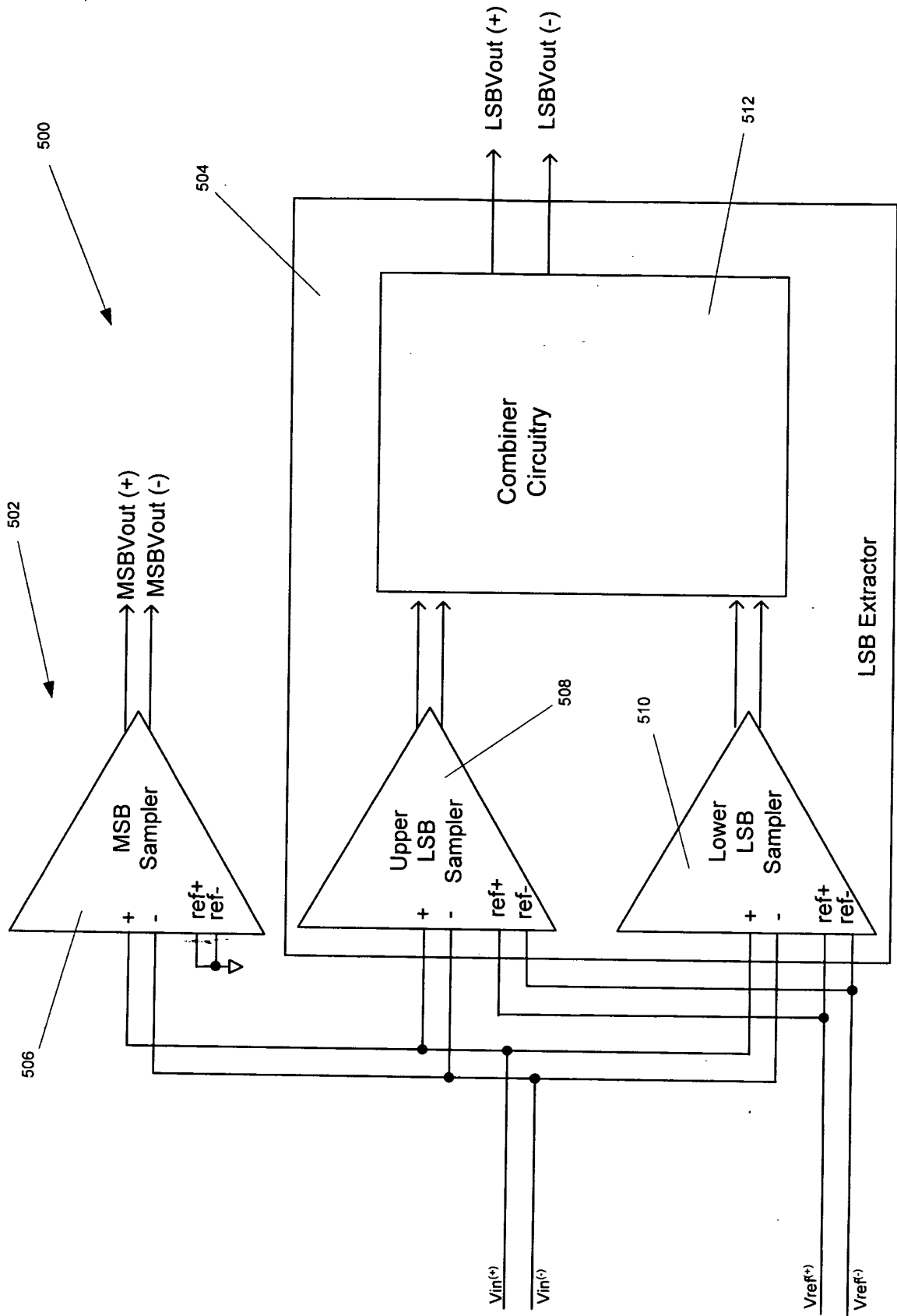


Figure 5A

Differential Logic Signal Level Binary Values

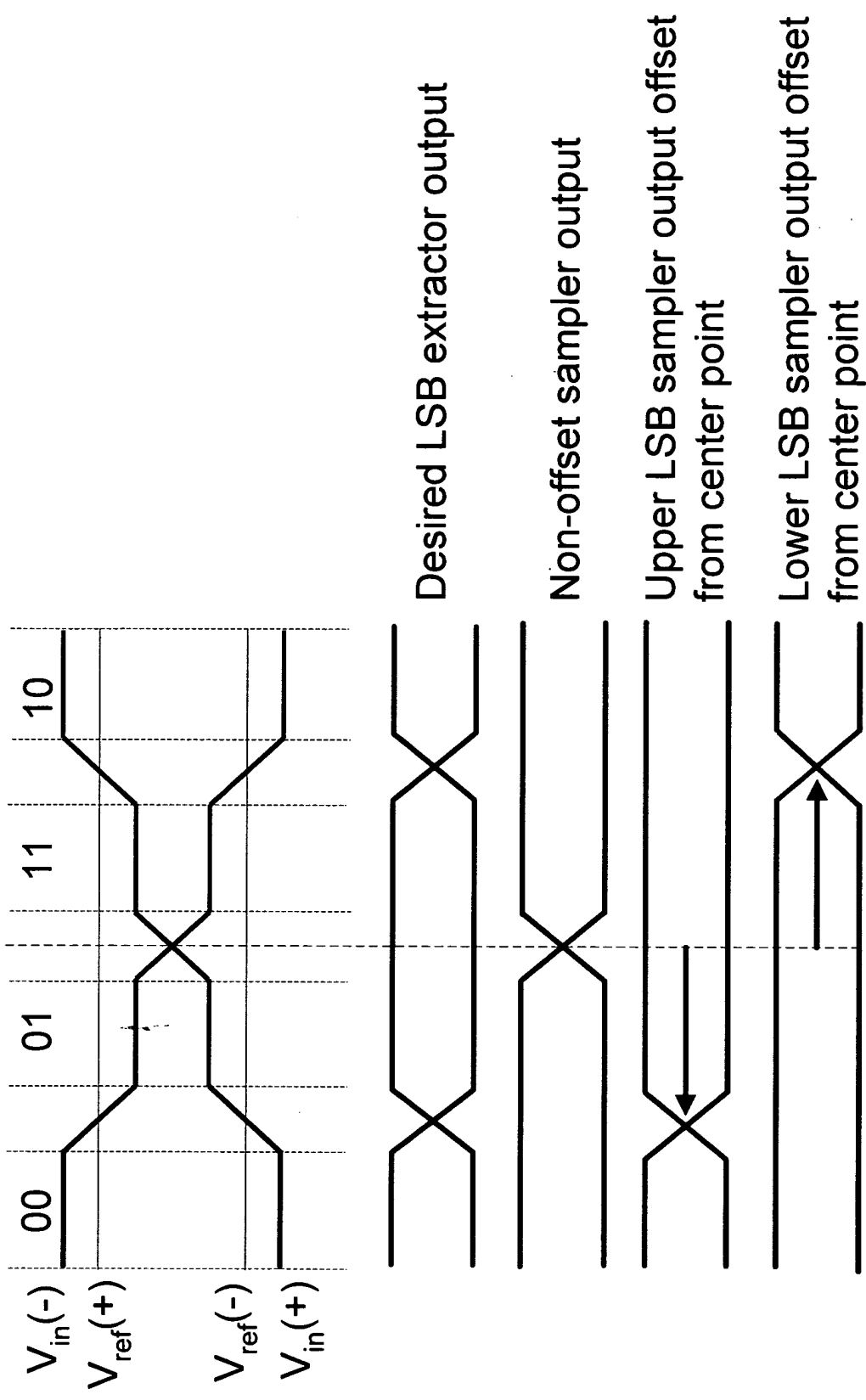


Figure 5B

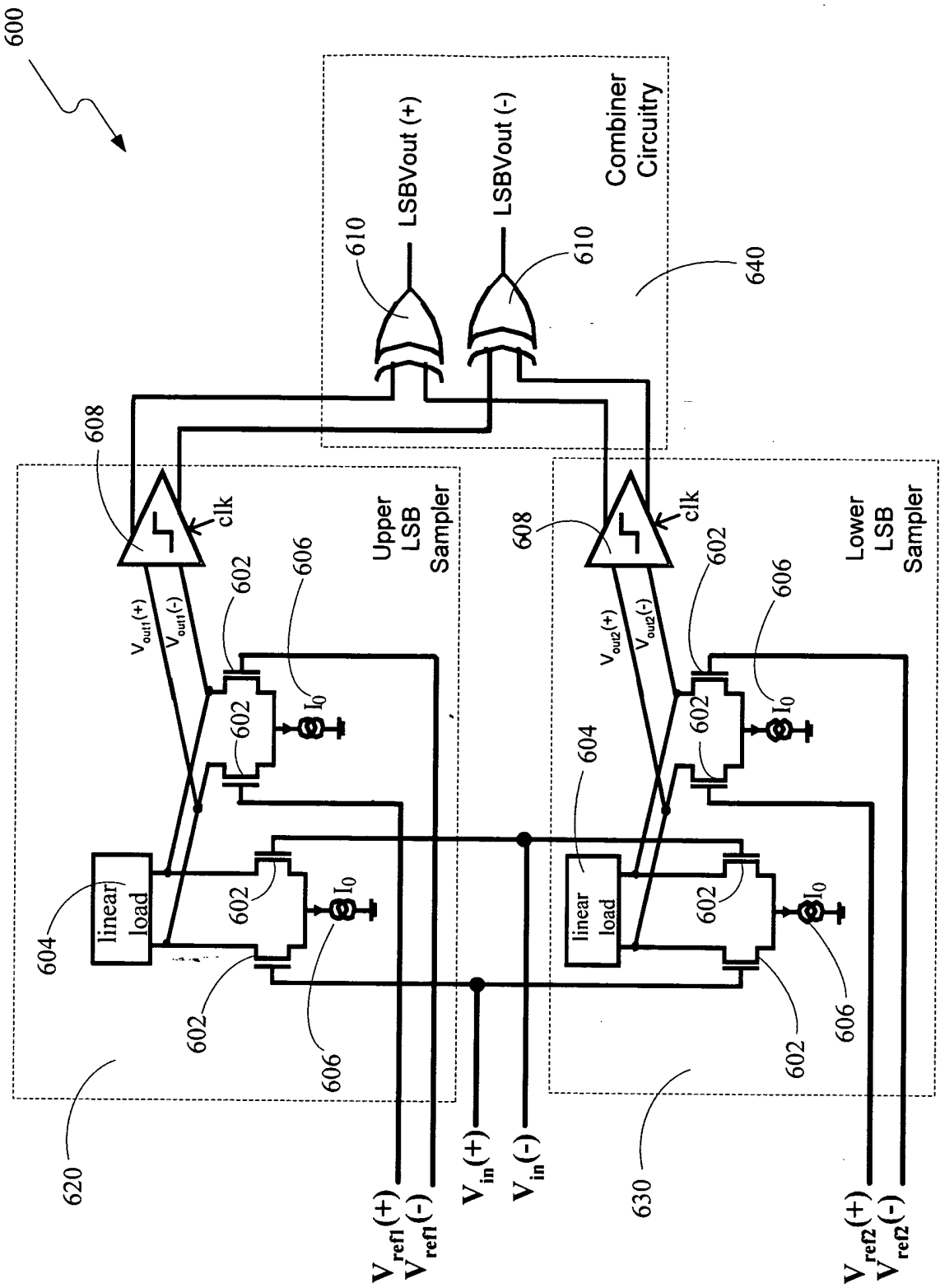


Figure 6

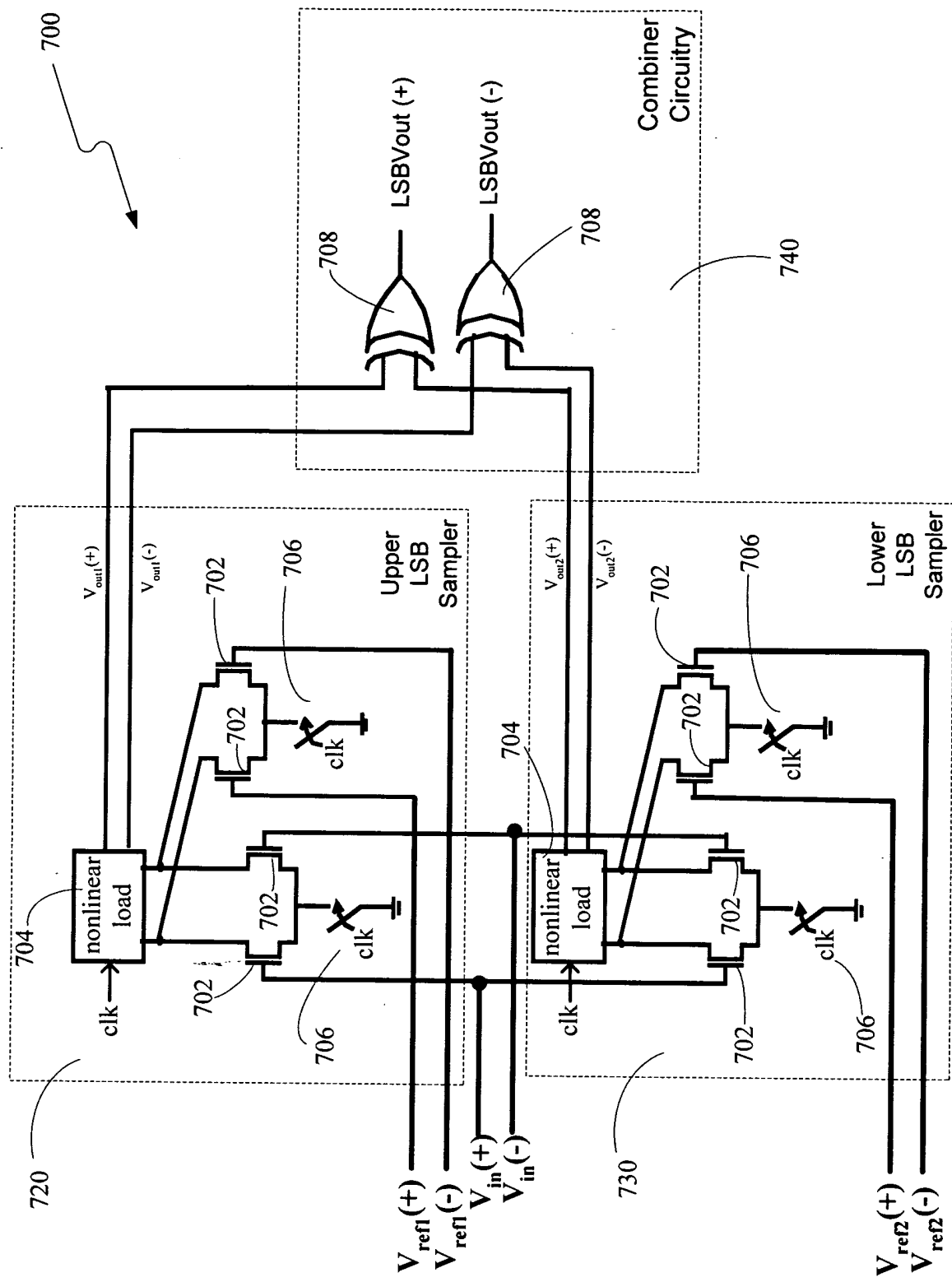


Figure 7

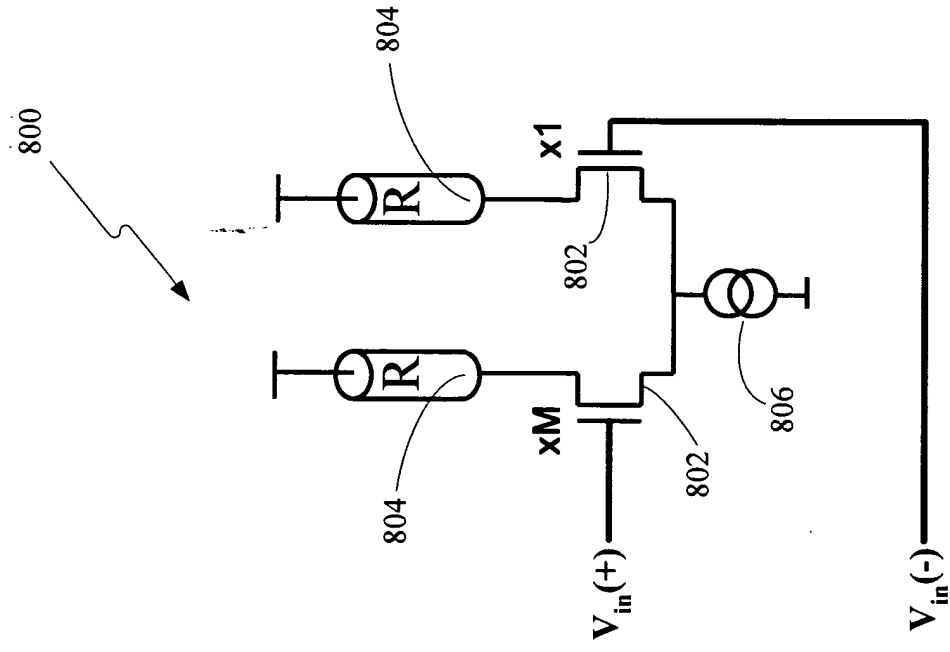


Figure 8A

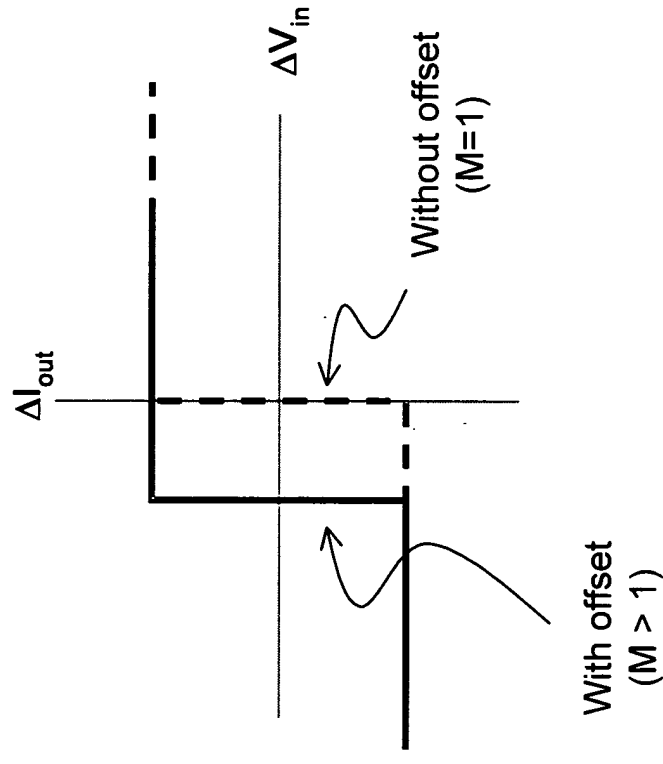


Figure 8B

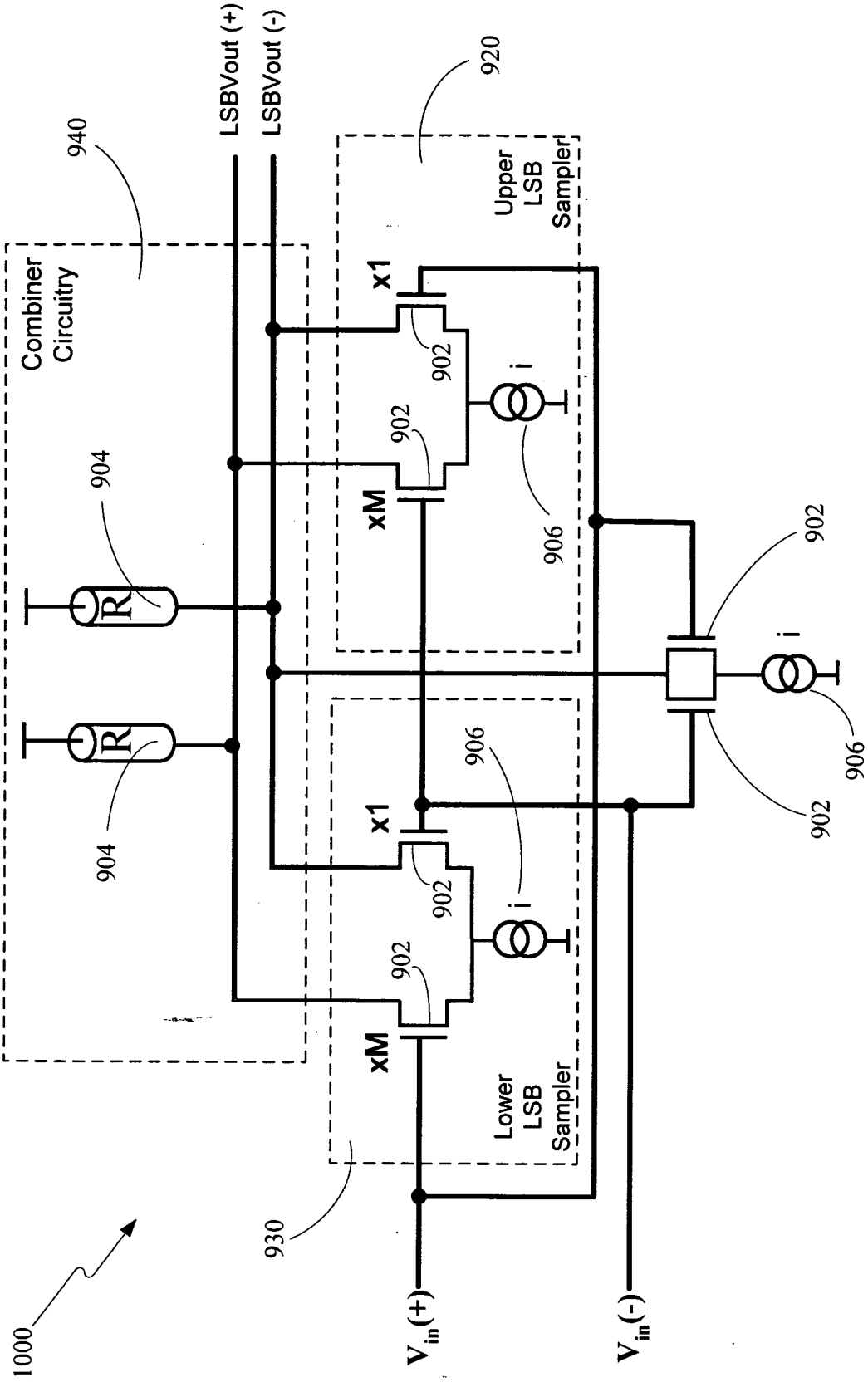


Figure 9

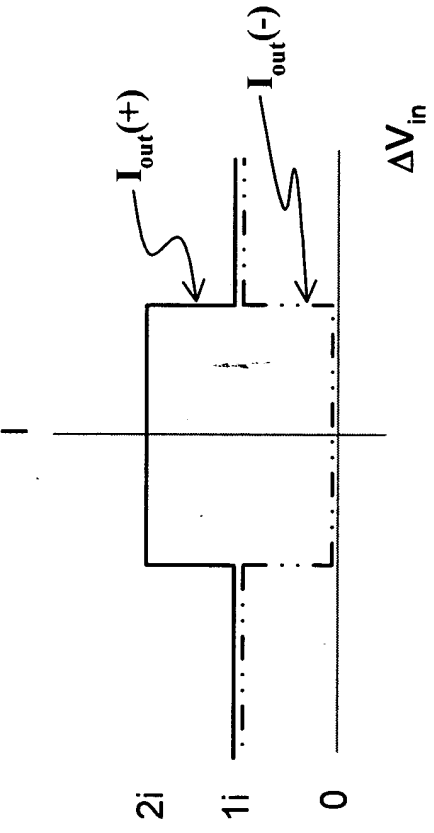


Figure 10A

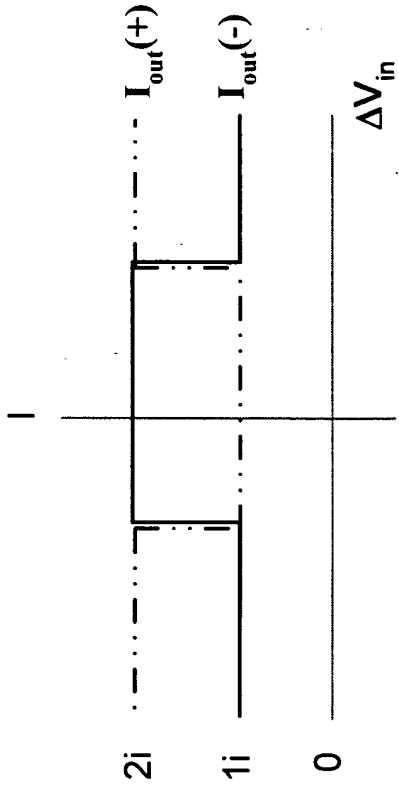


Figure 10B

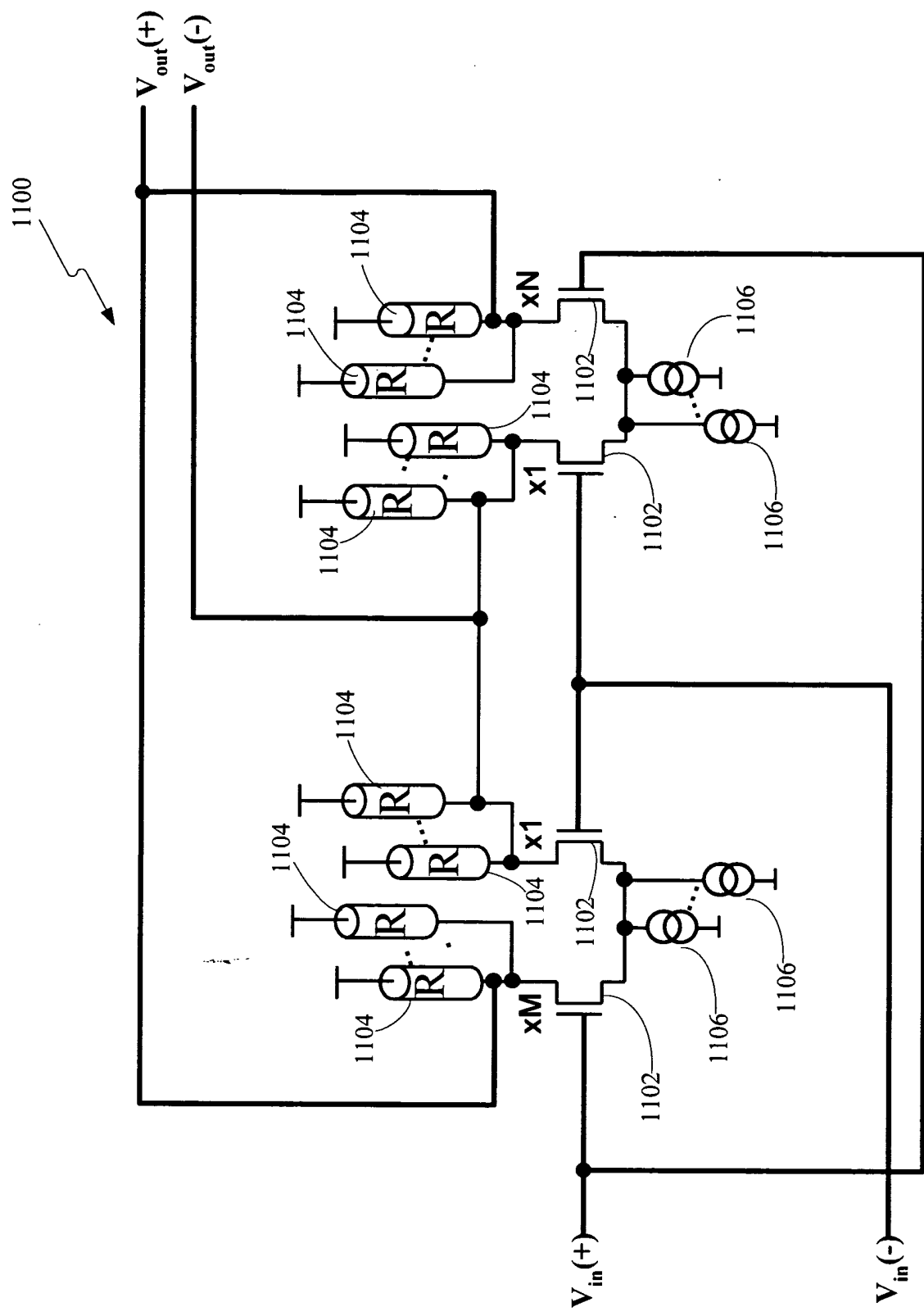


Figure 11

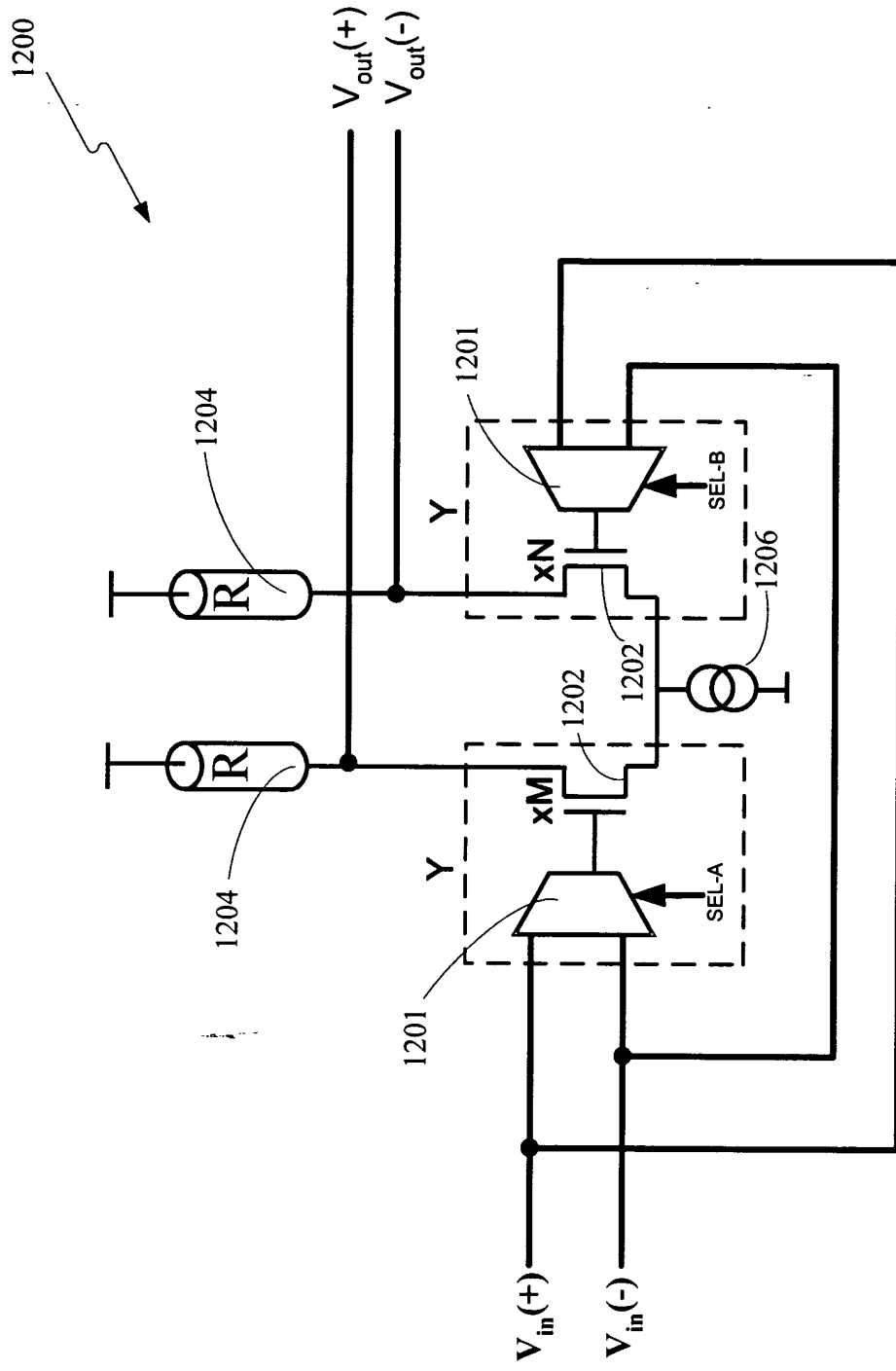


Figure 12

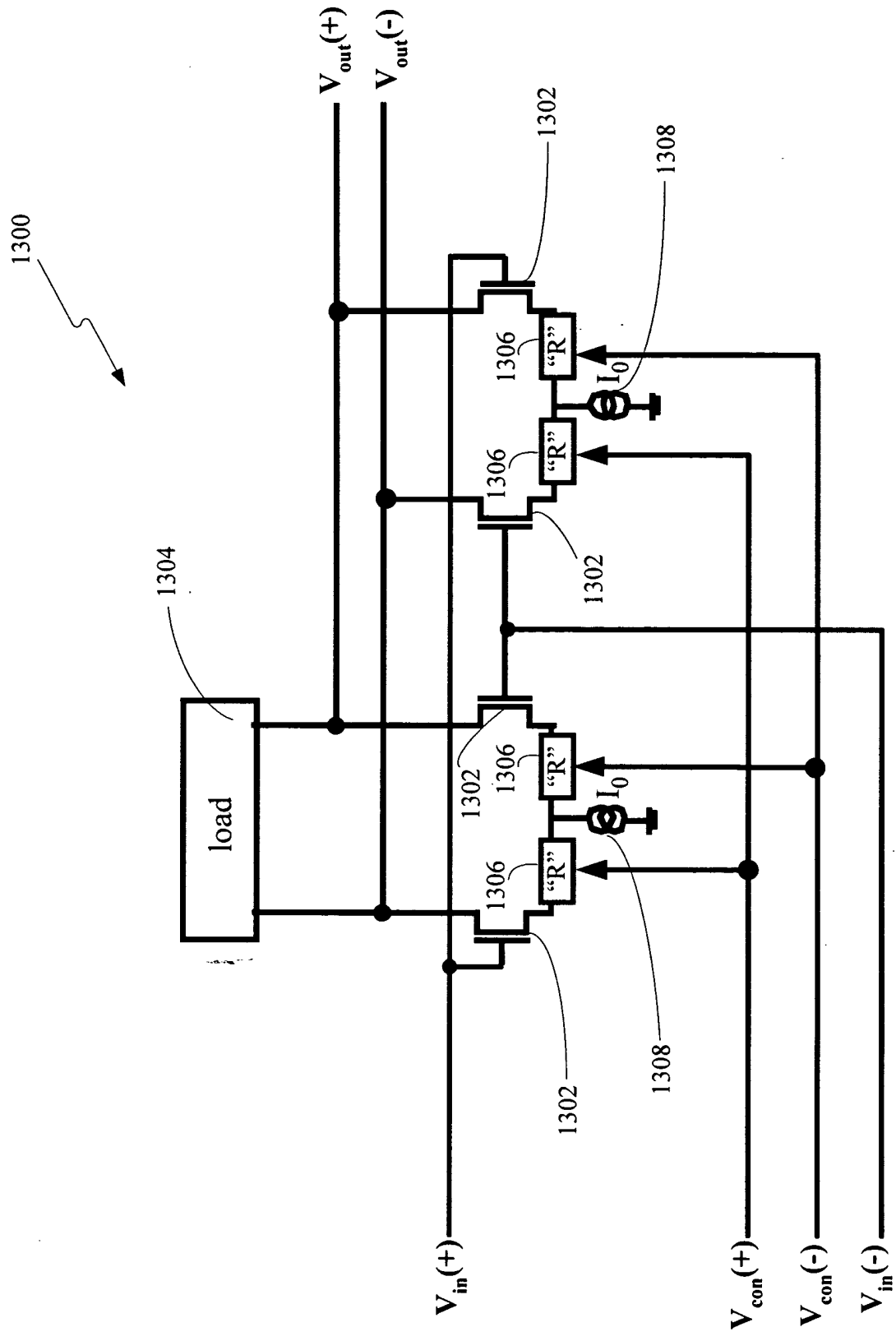


Figure 13

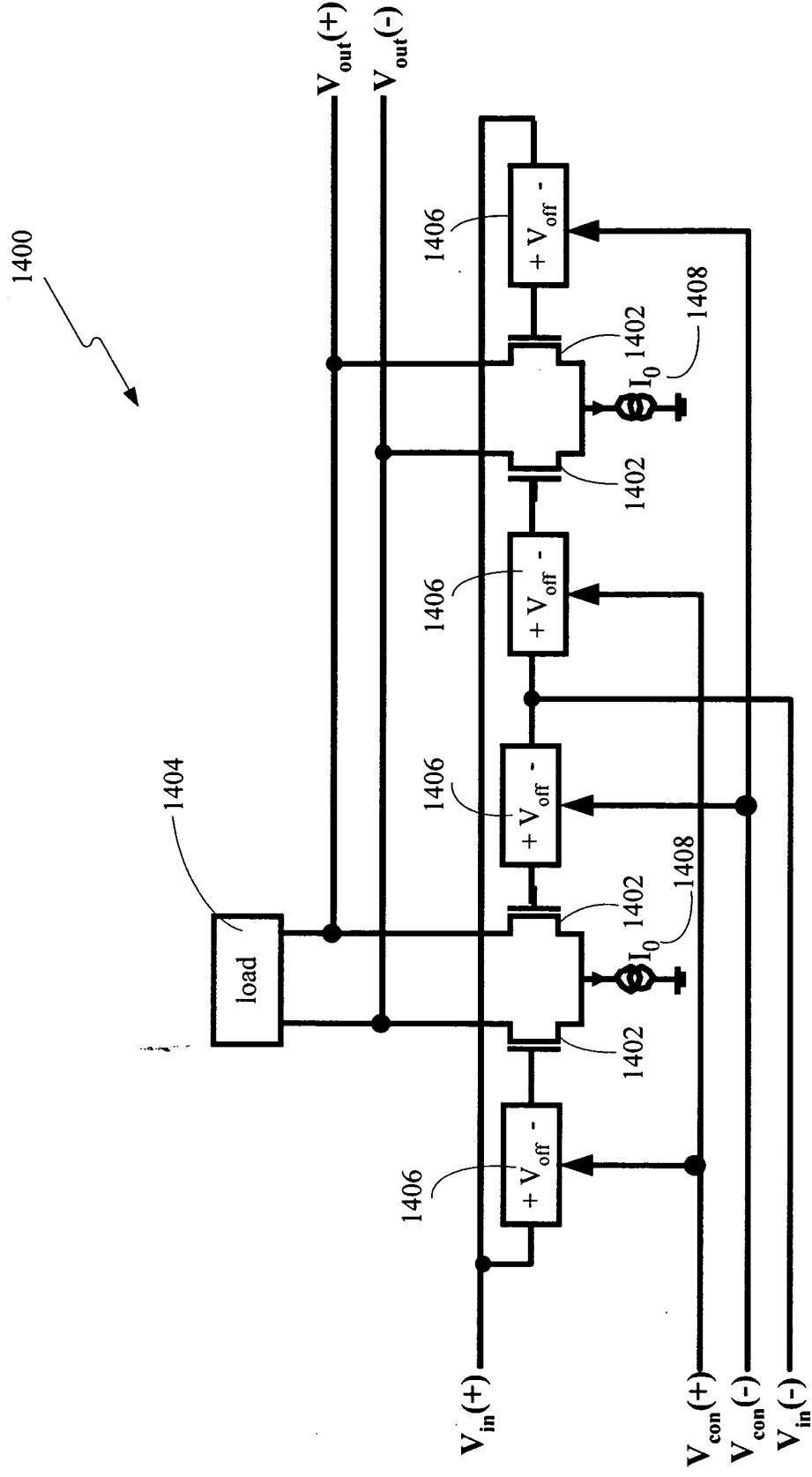


Figure 14A

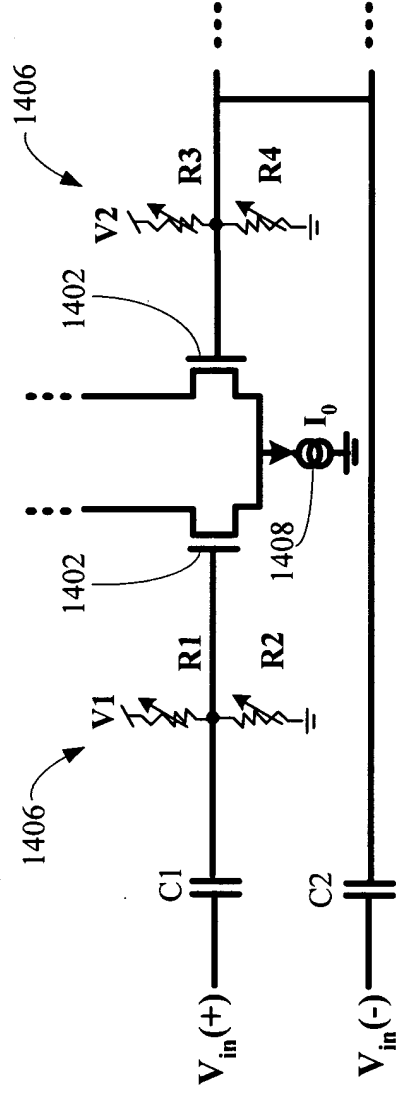


Figure 14B

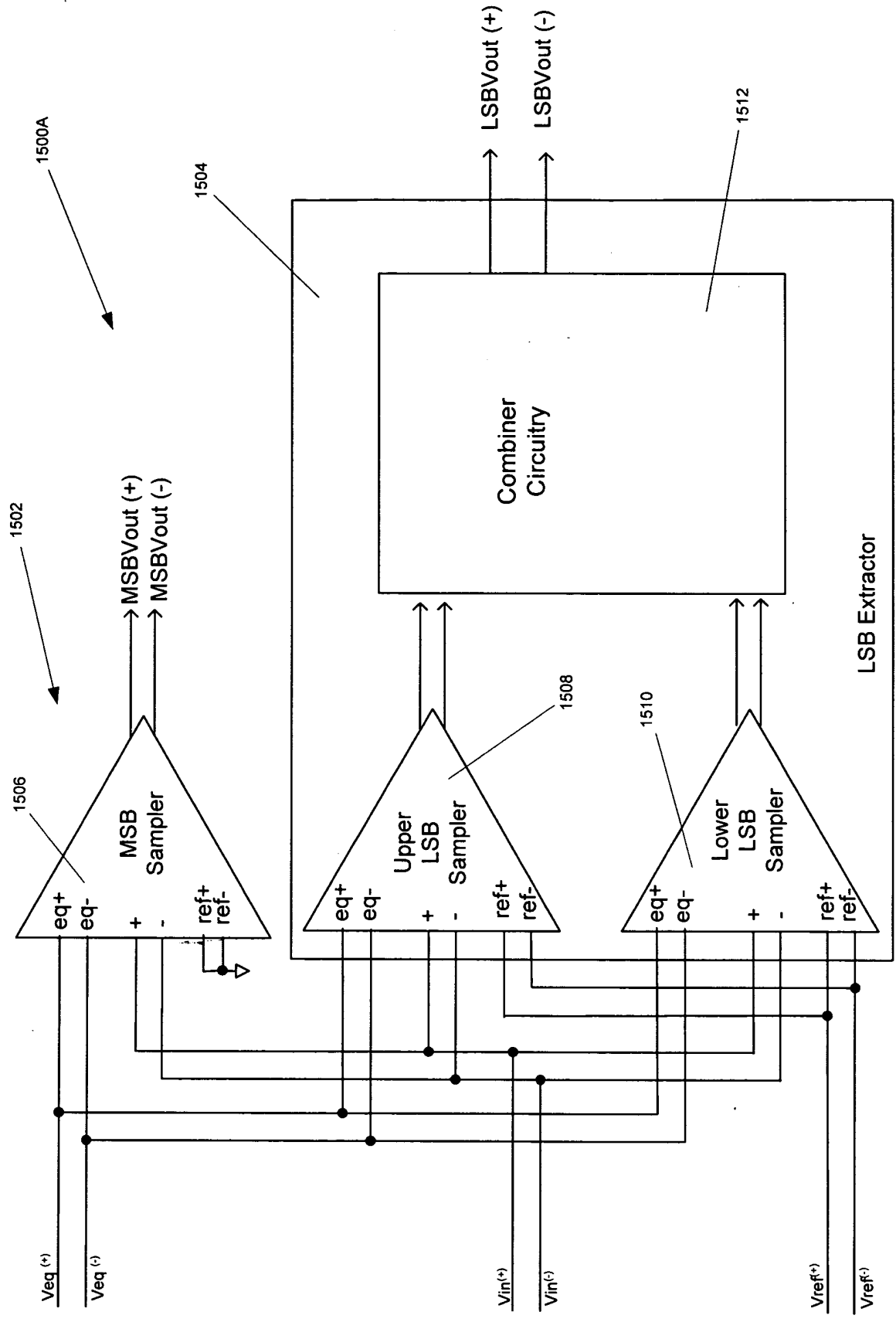


Figure 15A

1500B

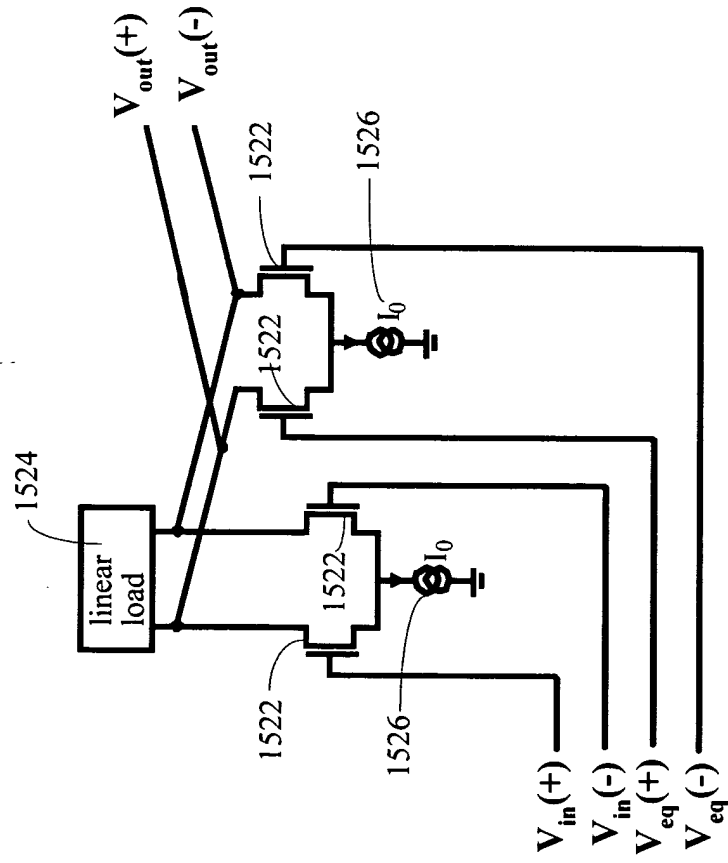


Figure 15B

1500C

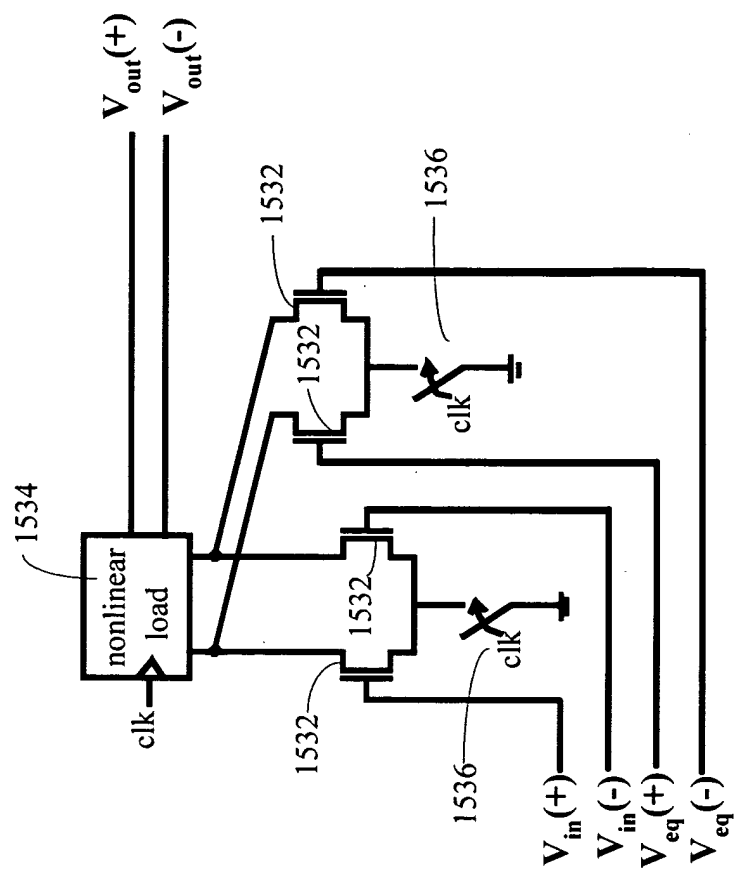


Figure 15C

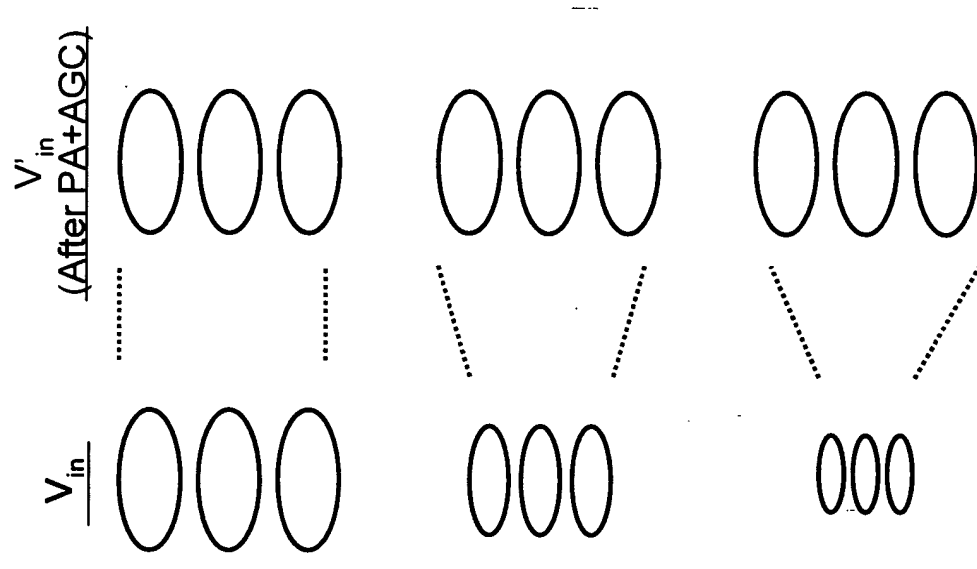


Figure 16B

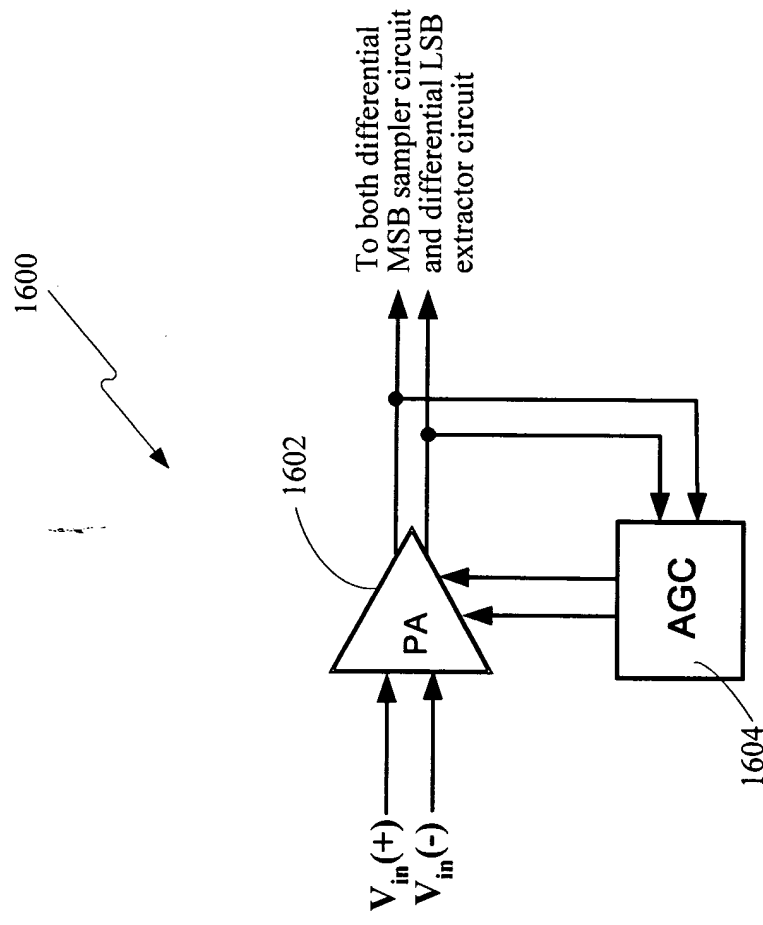


Figure 16A

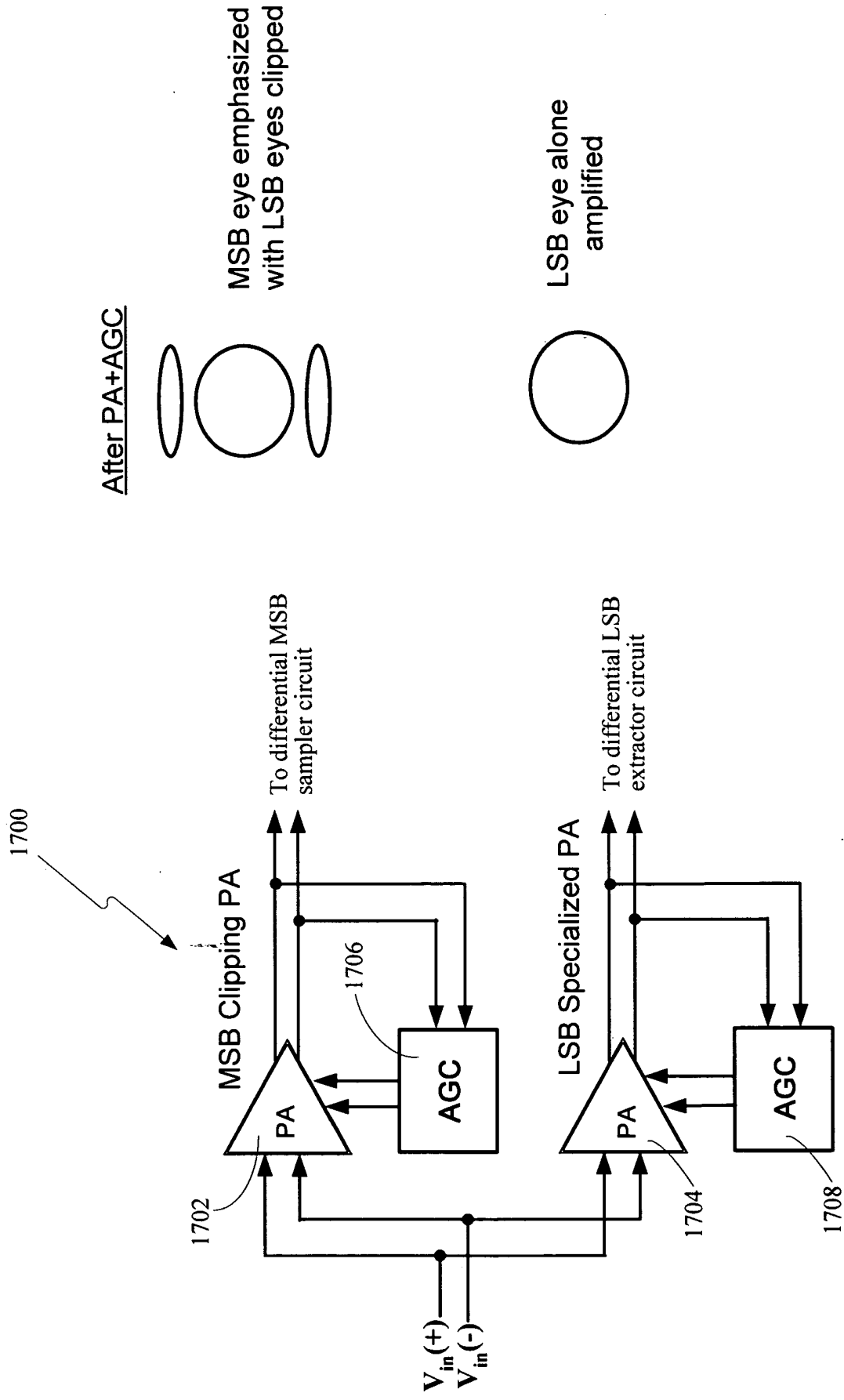


Figure 17A

Figure 17B

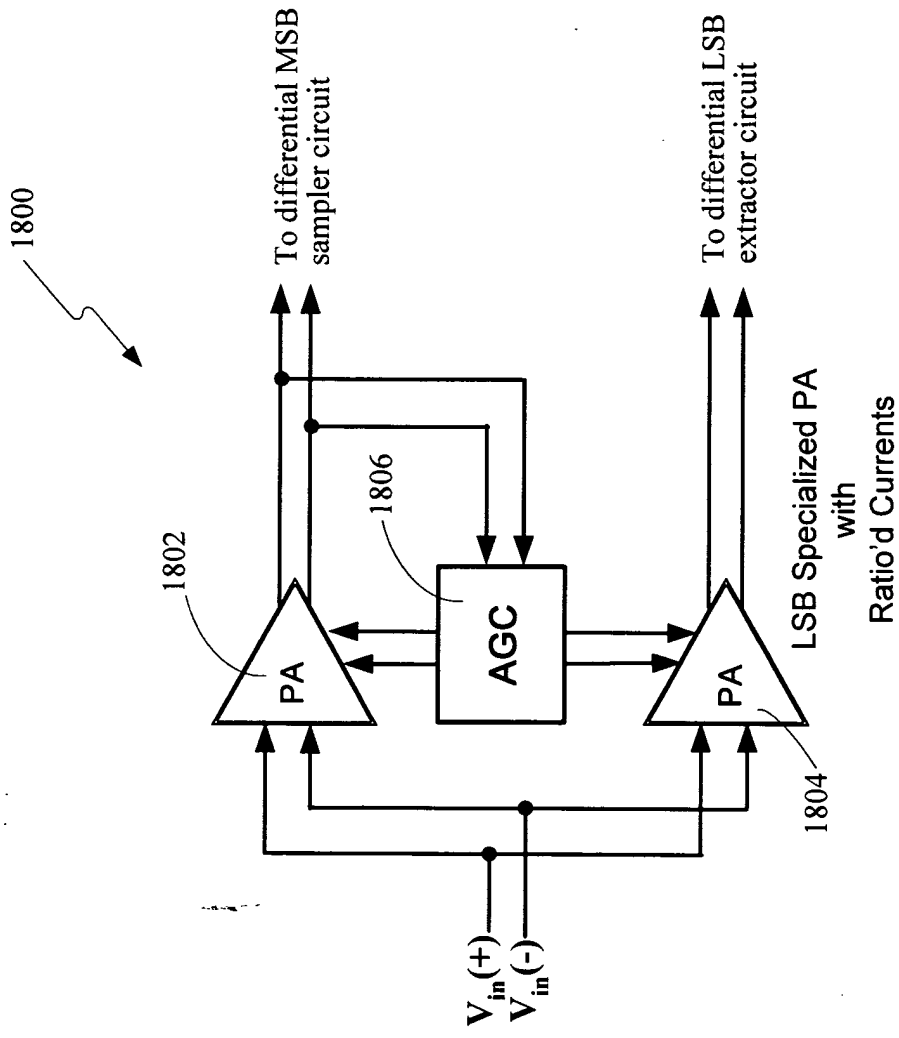


Figure 18

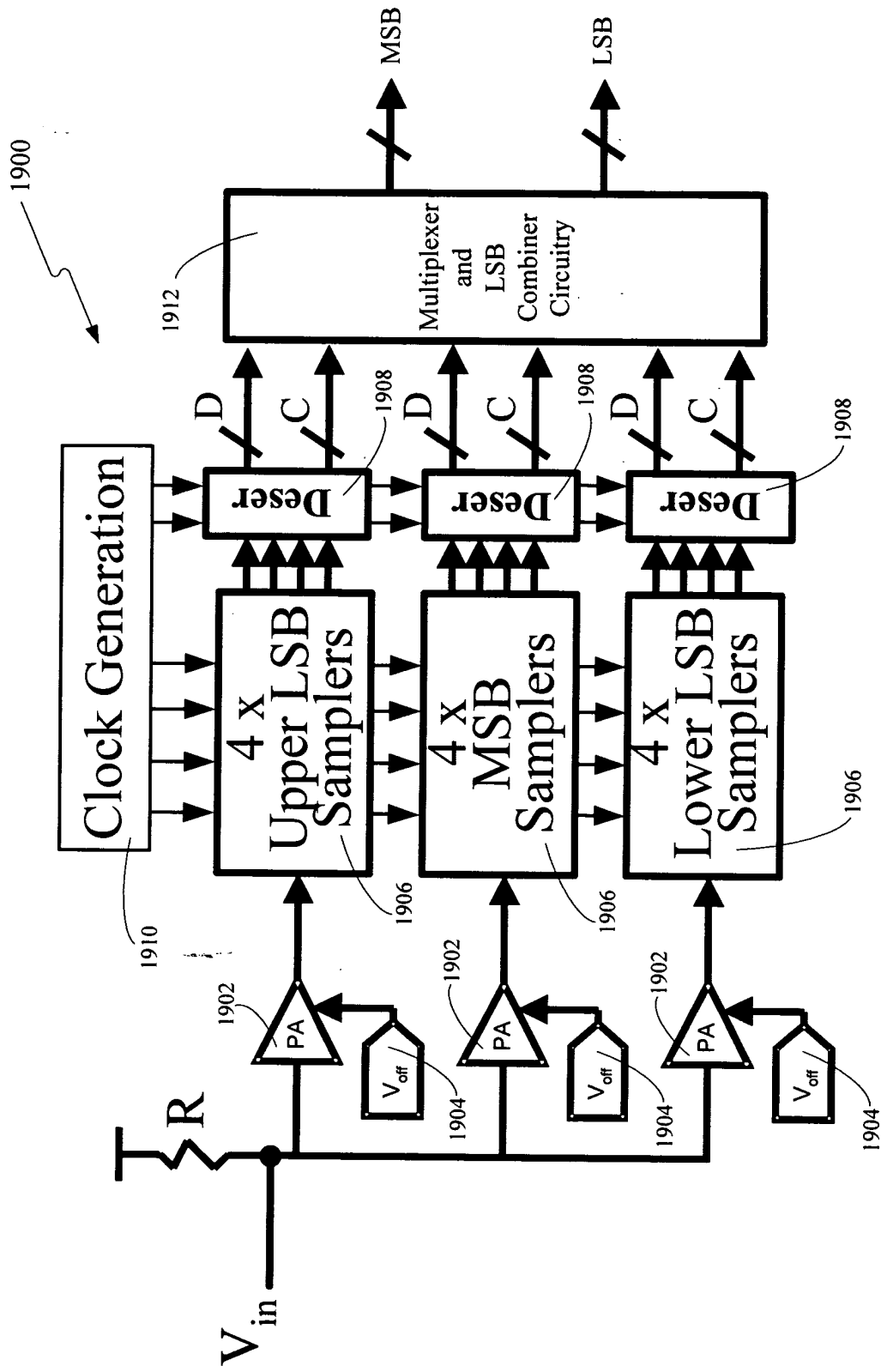


Figure 19

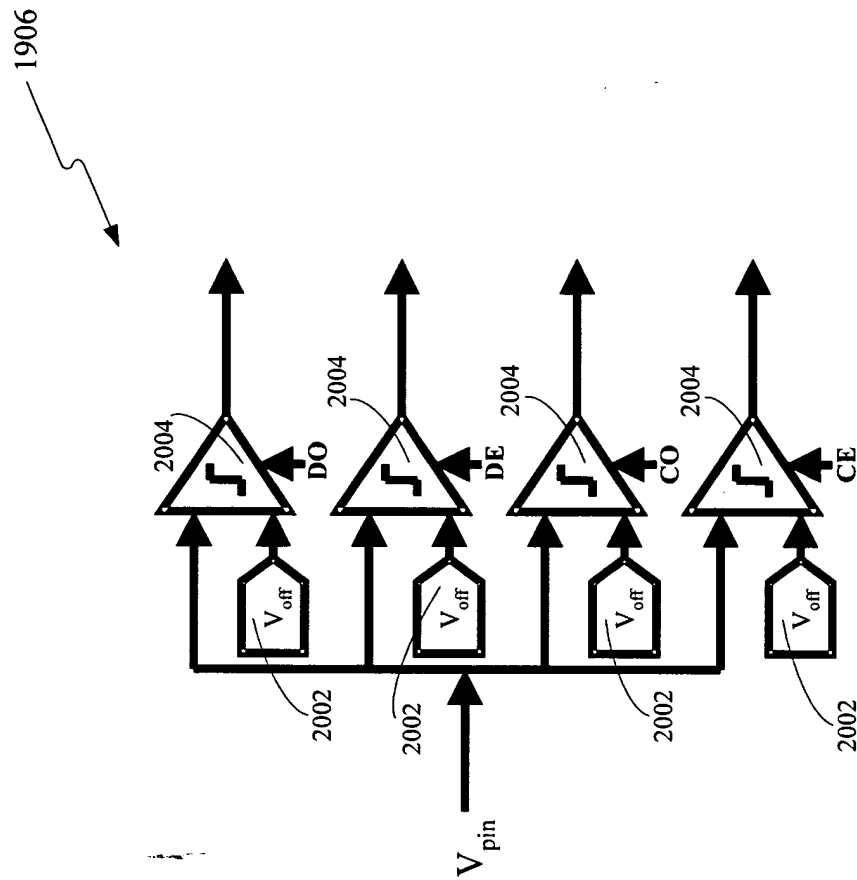


Figure 20

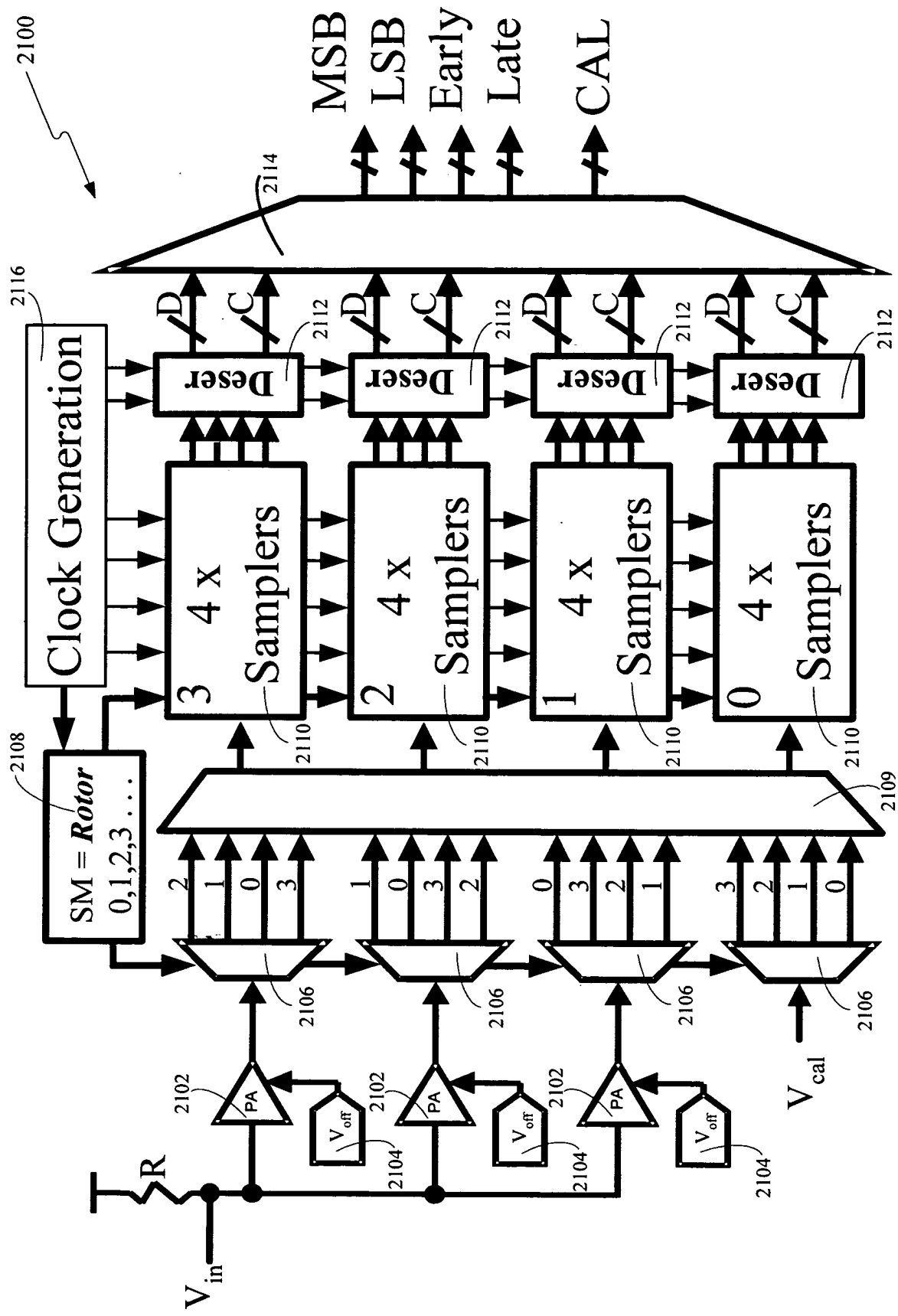


Figure 21

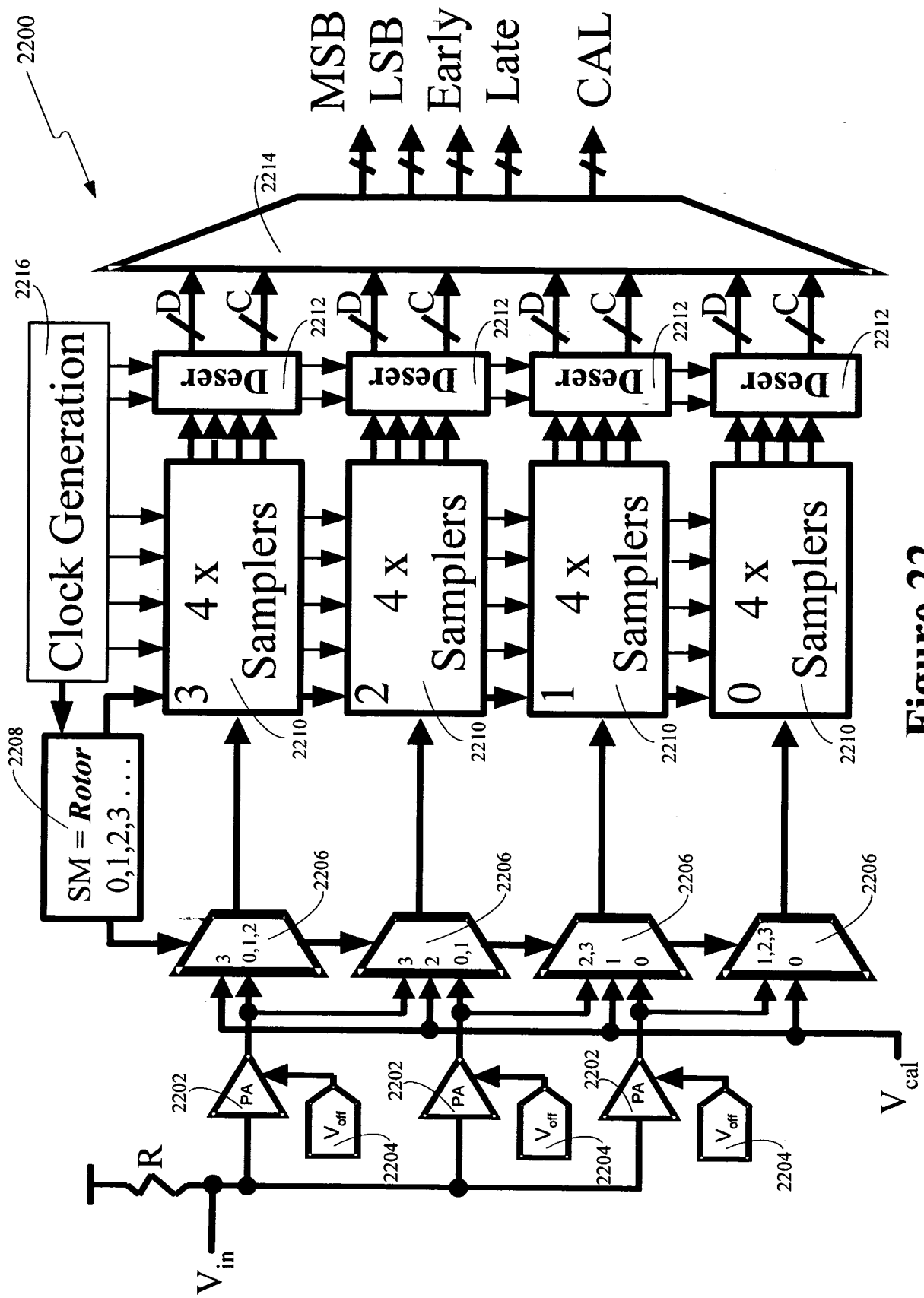


Figure 22

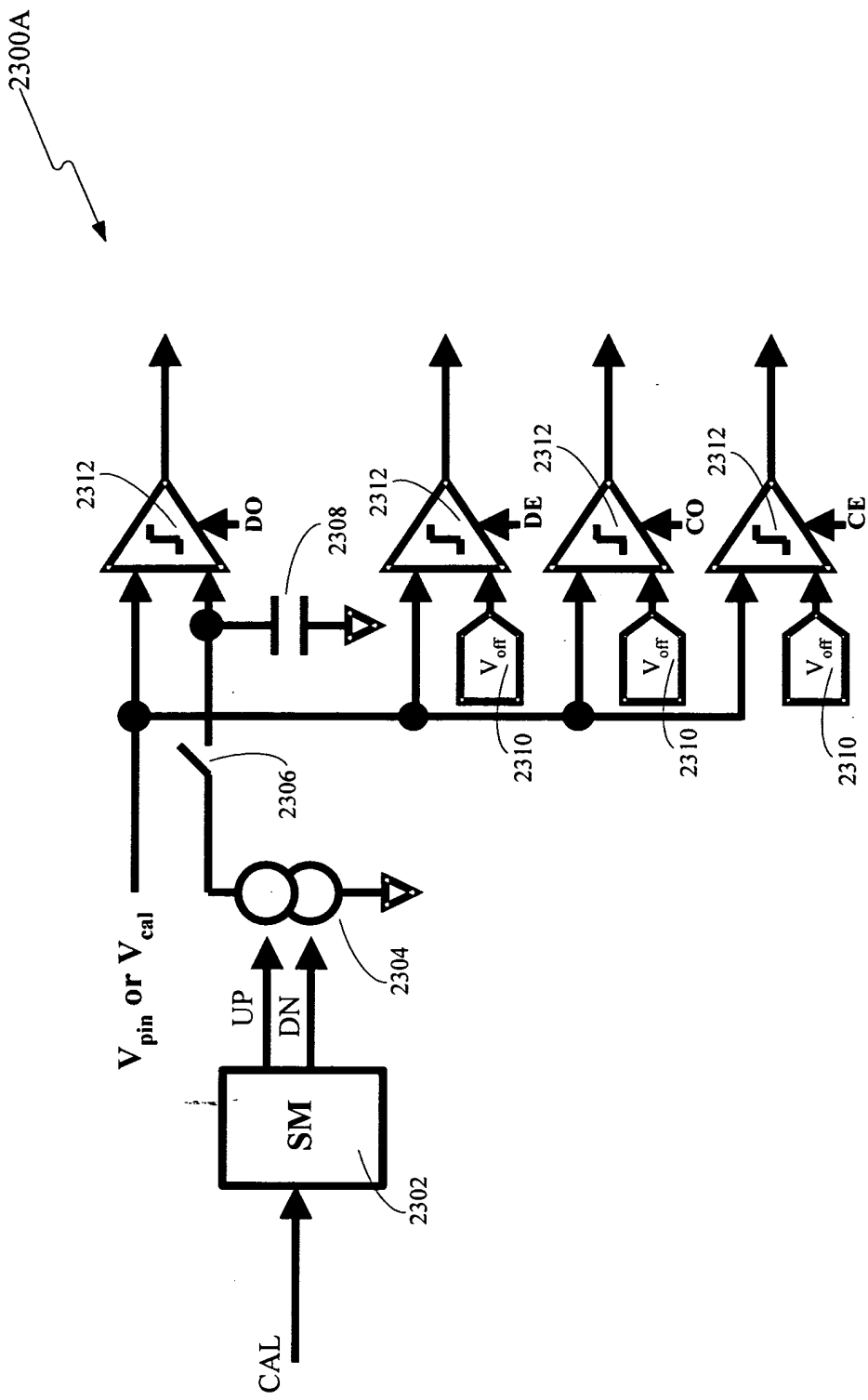


Figure 23A

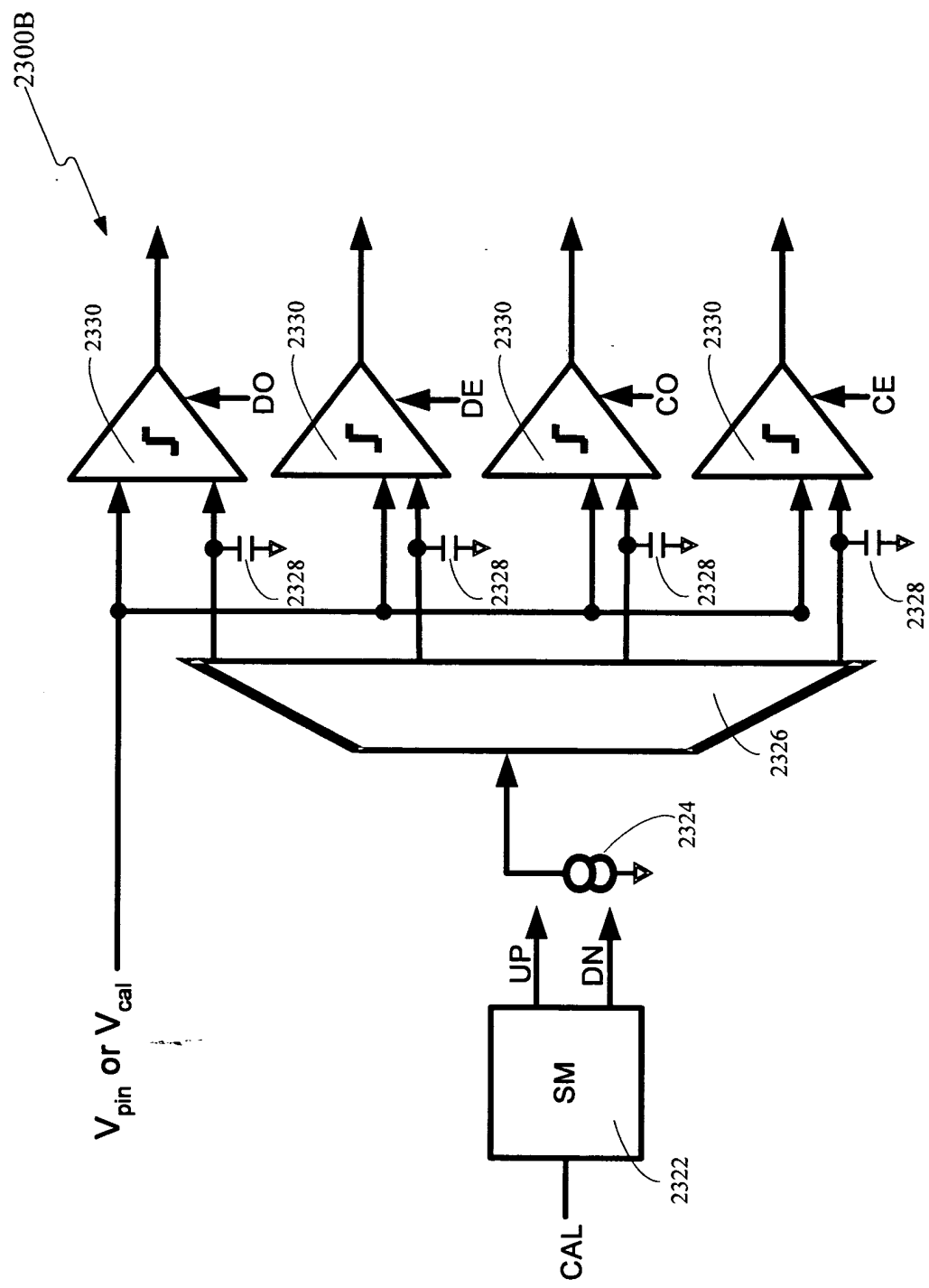


Figure 23B

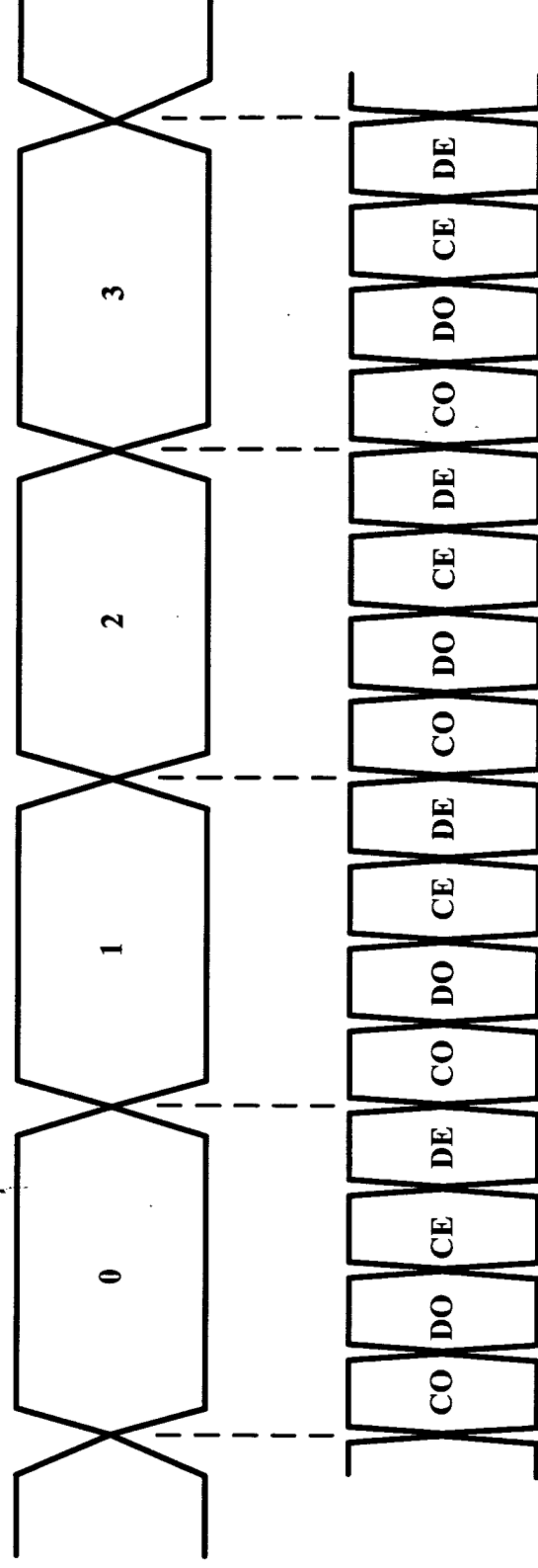


Figure 24